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Abbas et al.

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[54] **ELECTRICALLY ERASABLE FLOATING GATE FET MEMORY CELL**

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[52] **U.S. Cl.** **357/23,** 357/41

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[58] **Field of Search** ..... 317/235 B, 235 G

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[57] **ABSTRACT**

A read-mostly memory cell is disclosed comprising a floating gate avalanche injection field effect transistor storage device equipped with an erasing electrode. The memory portion of the erasable storage devices comprises a P channel FET having a floating polycrystalline silicon gate separated from an N-doped substrate by a layer of silicon dioxide. The erasing portion of the device comprises an erasing electrode separated from the polycrystalline silicon floating gate by a thermally grown layer of silicon dioxide having a leakage characteristic which is low in the presence of low electrical fields and high in the presence of high electrical fields. The floating gate is heavily doped with boron which also partially dopes the thermally grown silicon dioxide layer. The floating gate is charged negatively by avalanche breakdown of the FET drain while the erase gate is grounded to the substrate. The floating gate is discharged (erased) upon the application of a positive pulse to the erase electrode with respect to the semiconductor substrate causing electrodes on the charged floating gate to leak through the thermal oxide to the erasing electrode.

6 Claims, 3 Drawing Figures